IN THE CLAIMS

Please cancel claims 16-21 without prejudice and accept amended claims 1, 5-7 and 10-11 as follows:

1. (currently amended) A memory cell, comprising:

a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance;

a channel region defined between the source region and the drain region;

a first charge storage layer formed on the channel region adjacent the source region;

a second charge storage layer formed on the channel region adjacent the drain region;

a gate ~~insulting~~ insulating layer formed on the channel region between the first and second charge storage layers; and

a gate electrode formed on the gate insulating layer and the first and second charge storage layers, wherein the gate electrode comprises a gate sidewall pattern formed on each of the first and second charge storage layers, the gate sidewall pattern comprising a lower sidewall pattern and an upper sidewall pattern formed on the lower sidewall pattern.

2. (original) The memory cell as recited in claim 1, wherein the first and second charge storage layers each include a tunnel oxide layer, a charge trapping layer and

a blocking insulating layer in a stacked formation.

3. (original) The memory cell as recited in claim 1, wherein the gate insulating layer has an equivalent oxide thickness less than a thickness of each one of the first and second charge storage layers.

4. (original) The memory cell as recited in claim 1, wherein the gate insulating layer comprises sidewalls that are aligned with sidewalls of the first and second charge storage layers.

5. (currently amended) The memory cell as recited in claim 1, wherein the gate electrode further comprises:

a gate pattern formed on the gate insulating layer~~; and~~

~~a gate sidewall pattern formed on each of the first and second charge storage layers~~.

6. (currently amended) A memory cell, comprising:

a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance;

a channel region defined between the source region and the drain region;

at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first position is

adjacent the source region and the second position is adjacent the drain region;

a gate ~~insulting~~ insulating layer formed on the channel region between the at least two charge storage layers;

a gate pattern formed on the gate ~~insulting~~ insulating layer;

at least one lower sidewall pattern formed on at least one of the at least two charge storage layers; and

at least one upper sidewall pattern formed on the at least one lower sidewall pattern, wherein the at least one upper sidewall pattern electrically contacts the at least one lower sidewall pattern and the gate pattern.

7. (currently amended) The memory cell as recited in claim 6, wherein the at least two charge storage layers each include a tunnel oxide layer, a charge trapping layer and a blocking ~~insulting~~ insulating layer.

8. (original) The memory cell as recited in claim 6, wherein the gate insulating layer has an equivalent oxide thickness less than a thickness of each one of the at least two charge storage layers.

9. (original) The memory cell as recited in claim 6, wherein the gate insulating layer comprises sidewalls that are aligned with sidewalls of the at least two charge storage layers.

10. (currently amended) A memory cell, comprising:

a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance;

a channel region defined between the source region and the drain region;

at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first position is adjacent the source region and the second position is adjacent the drain region;

a gate ~~insulting~~ insulating layer formed on the channel region between the at least two charge storage layers;

a gate pattern formed on the gate ~~insulting~~ insulating layer;

at least one lower sidewall pattern formed on at least one of the at least two charge storage layers; and

at least one upper sidewall pattern formed on the at least one lower sidewall pattern, wherein the at least one lower sidewall pattern is electrically insulated from the at least one upper sidewall pattern and the gate pattern.

11. (currently amended) The memory cell as recited in claim 10, wherein the at least two charge storage layers each include a tunnel oxide layer, a charge trapping layer and a blocking ~~insulting~~ insulating layer.

12. (original) The memory cell as recited in claim 10, wherein the gate insulating layer has an equivalent oxide thickness less than a thickness of each one of the at least two charge storage layers.

13. (original) The memory cell as recited in claim 10, further comprising at least one inter-gate insulating layer interposed between the at least one lower sidewall pattern and the at least one upper sidewall pattern.

14. (original) The memory cell as recited in claim 10, wherein the gate insulating layer comprises sidewalls aligned with sidewalls of the at least two charge storage layers.

15. (original) The memory cell as recited in claim 10, wherein a voltage is independently applied to the gate pattern and to the at least one lower sidewall pattern.

16. - 21. (canceled)